

QUERY CONTROL FORM

RTIS USE ONLY

Application No. 1008/199

Prepared by TW

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JACKET

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b. Applicant(s)	g. Disclaimer	l. Print Fig.	q. PTOL-85b
c. Continuing Data	h. Microfiche Appendix	m. Searched Column	r. Abstract
d. PCT	i. Title	n. PTO-270/328	s. Sheets/Figs
e. Domestic Priority	j. Claims Allowed	o. PTO-892	t. Other

SPECIFICATION

- a. Page Missing
- b. Text Continuity
- c. Holes through Data
- d. Other Missing Text
- e. Illegible Text
- f. Duplicate Text
- ☒ g. Brief Description
- h. Sequence Listing
- i. Appendix
- j. Amendments
- k. Other

CLAIMS

- a. Claim(s) Missing
- b. Improper Dependency
- c. Duplicate Numbers
- d. Incorrect Numbering
- e. Index Disagrees
- f. Punctuation
- g. Amendments
- h. Bracketing
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- k. Other

MESSAGE

Figure 8 is not described on Page 10

Please verify

Thank You

initials *Tw*

RESPONSE

Corrected

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Brief Description of the Drawings

The foregoing and further and more specific objects and advantages of the present invention will become readily apparent to those skilled in the art from the following detailed description of a preferred embodiment thereof taken in conjunction with the drawings, in which:

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FIGs. 1-⁸/₇ illustrate cross-sectional views of the steps in fabricating a tiered structure according to the present invention.

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Detailed Description of the Preferred Embodiments

15 In developing a tiered structure, such as a T-gate structure, according to the present invention, the challenge lies in creating a tiered structure using only positive resists composed of polymeric materials having a low to medium molecular weight. In order to accomplish this, several issues must be overcome. First, resist compatibility must be taken into account. Low to
20 medium molecular weight (MW) i-line and deep ultra violet (DUV) resists tend to intermix when other layers are coated on top of them. Use of these resists as the bottom resist layer must somehow avoid intermixing. Second, resist/developer compatibility must be examined. Resists and developers must be chosen in such a way to affect only the layer(s) intended. Third,
25 bake temperature compatibility must be dealt with. As the stack is built, care